PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

HIKITA et al. Art Unit: 2815

Application No.: 09/496,183 Examiner: CRUZ, L.

Filed: February 2, 2000 Attorney Dkt. No.: 103213-09038

For: SEMICONDUCTOR DEVICE AND SEMICONDUCTOR CHIP FOR USE THEREIN

15#/amdtC 3/19/2

RESPONSE UNDER 37 CFR § 1.121

Commissioner for Patents
Washington, D.C. 20231

Date: March 12, 2002

Sir:

In response to the outstanding Office Action dated December 14, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claim 12 without prejudice.

Please amend claims 1, 3 and 10 as follows. Pursuant to 37 C.F.R. § 1.121, as amended, a copy of the marked-up version of the original claims is attached to this Response showing the changes made therein.

1. (Twice Amended) A semiconductor device comprising a first semiconductor chip and a second semiconductor chip superposed on and bonded to a surface of the first semiconductor chip,

wherein, in a chip bonding region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, chip

connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips,

wherein, on the second semiconductor chip, chip connection portions are arranged so as to fit the chip connection portions arranged on the first semiconductor chip at least for one of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

C1 cont.

3. (Twice Amended) A semiconductor chip having, on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips,

C2

wherein, in the chip bonding region, chip connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a

distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

C2 cont.

10. (Twice Amended) A semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips,

C3

wherein, in the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are arranged along an edge of the chip connection region, and

wherein the chip connection portions are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

REMARKS

The Office Action dated December 14, 2001, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claim 12 has been cancelled without prejudice. Claims 1, 3 and 10 have been amended. No new matter has been added by the amendments made herein. Accordingly, claims 1-5, 10 and 11 are pending the present application and are respectfully submitted for consideration.

Claims 1-5 and 10-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wenzel et al. (U.S. Patent No. 6,150,724, hereinafter "Wenzel"). As mentioned above, claim 12 has been cancelled without prejudice, and therefore the rejection with respect to this claim is now moot. As for claims 1-5, 10 and 11, Applicants respectfully submit that each of these claims recites subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1, upon which claim 2 is dependent, recites a semiconductor device comprising a first semiconductor chip and a second semiconductor chip superposed on and bonded to a surface of the first semiconductor chip. In a region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, the chip connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips. In addition, on the second semiconductor chip, the chip connection portions are arranged so as to fit the chip connection portions arranged on the first semiconductor chip at least for one of the

plurality of predetermined types of semiconductor chips. Furthermore, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Claim 3, upon which claims 4-5 are dependent, recites a semiconductor chip having, on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips. In the chip bonding region, the chip connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips. Additionally, the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Claim 10, upon which claims 11-12 are dependent, recites a semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips. In the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are arranged along an edge of the chip connection region. Furthermore, the chip connection portions are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

Accordingly, the present invention provides a semiconductor device having a chip-on-chip structure that allows easy production of various types of semiconductor devices as a whole, and further provides a semiconductor chip for use in a semiconductor device. As such, the present invention provides an efficient and cost effective method and device for upgrading an existing system, such as increasing the capacity of a memory, increasing the number of conversion bits of A/D conversion device, or increasing the number of processing bits of a CPU.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims, and therefore fails to provide the advantages which are provided by the present invention.

Wenzel discloses a bump-bonded multi-IC flip-chip semiconductor device 100. The device 100, as illustrated in Figure 5 of Wenzel, has a mother integrated circuit or chip 102 and a daughter integrated circuit or chip 104. The active surface of the mother chip 102, which contains active circuitry, faces the active surface circuitry of the daughter integrated circuit 104. In other words, the active surface of both ICs 102 and 104 are facing one another. The conductive bumps 108 are used to interconnect active circuitry and interconnect structures located on the mother integrated circuit 102 with active circuitry or conductive structures located on the daughter integrated circuit 104. The interconnected structure of the chips 102 and 104 is coupled to a ceramic, organic, or other package 106 through conductive connection bumps 110. Central bumps 108 are used to connect two or more integrated circuits to each other while peripheral bumps 110 are used to connect the mother chip 102 to the semiconductor package 106 to enable electrical connection of the ICs 102 and 104 to an external environment.

Applicants respectfully submit that each and every element recited in claims 1, 3 and 10 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicants respectfully submit that the semiconductor device having a chip-on-chip structure recited in the present claims is clearly distinct from that which is illustrated in Wenzel. It is submitted that Wenzel fails to disclose or suggest at least the limitation of "wherein the chip connection portions arranged on the first semiconductor

chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications."

As discussed above, Wenzel merely discloses a bump-bonded multi-chip flip-chip device 100 formed by manufacturing a mother chip 102 having a first set 207 of bumps 212 and a second set 209 of bump contact with conductive bumps 108 used to interconnect activity circuitry and interconnect structures located on the mother integrated circuit 102 with active circuitry or conductive structures located on the daughter integrated circuit 104. Although Wenzel discloses conductive bumps 108, Applicants respectfully submit that Wenzel does not disclose or suggest the limitation wherein the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along one of the opposite sides is shorter than a distance from the chip connection portions arranged along one of the opposite sides to the chip connection portions arranged along the other of the opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications. In other words, it is respectfully submitted that Wenzel

fails to disclose at least part of the chip connection portions arranged on the first semiconductor chip are common to a plurality of predetermined types of semiconductor chip. It is respectfully submitted that by using these common chip connection portions, it is possible to achieve connection with a plurality of types of semiconductor chip. Accordingly, Applicants respectfully submit that Wenzel fails to disclose and suggest each and every element recited in independent claims 1, 3 and 10 of the present application.

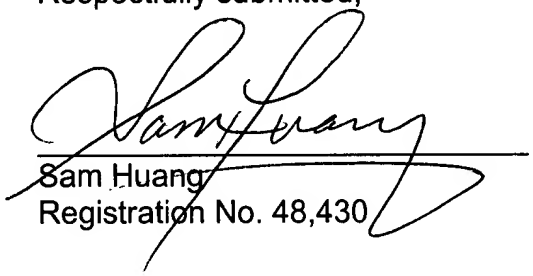
As for dependent claims 2, 4-5 and 11, Applicants submit that each of these claims recites subject matter which is neither disclosed nor suggested by Wenzel. In particular, each of claims 2, 4-5 and 11 depends from claims 1, 3 and 10, respectively. Therefore, each of these dependent claims incorporates each and every limitation recited within claims 1, 3 and 10, therein. Therefore, Applicants submit that each of claims 2, 4-5 and 11 also recites subject matter which is neither disclosed nor suggested by Wenzel for at least the reasons set forth above with respect to claims 1, 3 and 10.

In view of the above, Applicants respectfully submit that claims 1-5 and 10-11, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-5 and 10-11 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicants' undersigned Attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Enclosure: Marked-Up Copy of Original Claims